CLAIMS

What is claimed is:

1. An integrated circuit comprising:

circuitry;

a bond pad coupled to the circuitry and for interfacing the circuitry with an external circuit; and

a special contact pad coupled to the circuitry, the special contact pad for use only when testing the circuitry.

2. The integrated circuit of claim 1, wherein the special contact pad is smaller than the bond pad.

3. The integrated circuit of claim 1, wherein the special contact pad has a maximum dimension of approximately 10 microns.

4. The integrated circuit of claim 1, wherein the special contact pad is structured to receive a spring contact element.

5. The integrated circuit of claim 1, wherein the special contact pad is for communicating test data to the circuitry.

6. The integrated circuit of claim 1, wherein the special contact pad is for communicating data from the circuitry.

7. The integrated circuit of claim 1, wherein the special contact pad is for contacting a circuit node internal to the circuitry.

8. An integrated circuit comprising:

a plurality of circuits;

a plurality of bond pads each coupled to at least one of the plurality of circuits, the plurality of bond pads for interfacing the plurality of circuits with circuits external to the integrated circuit; and

a plurality of special contact pads each coupled to at least one of the plurality of circuits and providing an electrical contact for communicating with the plurality of circuits.

9. The integrated circuit of claim 8, wherein the bond pads are arranged in a first predetermined alignment and the special contact pads are arranged in a second predetermined alignment.

10. The integrated circuit of claim 8, wherein the bond pads are disposed along the periphery of the integrated circuit, and at least one of the special contact pads is not disposed on the periphery of the integrated circuit.

11. The integrated circuit of claim 8, wherein the bond pads are aligned in a grid pattern on the integrated circuit, and at least one of the special contact pads is not aligned in the grid pattern.

12. The integrated circuit of claim 8, wherein the bond pads are aligned in a lead-on-center configuration, and at least one of the special contact pads is not aligned in the lead-on-center configuration.

13. The integrated circuit of claim 8, wherein the special contact pads are smaller than the bond pads.

14. The integrated circuit of claim 8, further comprising a spring contact element attached to one of the special contact pads.

15. The integrated circuit of claim 8, wherein at least one of the special contact pad is electrically disposed between two of the plurality of circuits to monitor signals transmitted between circuits.

16. The integrated circuit of claim 8, wherein one of the special contact pads communicates test data to one of the circuits, and another one of the special contact pads communicates an output of the circuit.

17. The integrated circuit of claim 8, wherein one of the special contact pads communicates test data to the one of the circuits, and one of the bond pads communicates an output of the circuit.

18. The integrated circuit of claim 8, wherein one of the bond pads communicates test data to one of the circuits, and one of the special contact pads communicates an output of the circuit.

19. The integrated circuit of claim 8, wherein in a first mode of operation one of the special contact pads communicates data to one of the circuits, and in a second mode of operation the special contact pads communicates data from the circuit.

20. The integrated circuit of claim 8, wherein one of the plurality of circuits is an embedded memory array, and the special contact pads communicates address and test data to the embedded memory array.

21. The integrated circuit of claim 8, wherein one of the plurality of circuits includes programmable circuitry, and the special contact pads are for communicating signals for programming the programmable circuitry.

22. The integrated circuit of claim 8, wherein the bond pads are structured to be connected to external circuitry by bonding wires, and the special contact

pads are not structured to be connected to external circuitry by bonding wires.

23. The integrated circuit of claim 8, wherein the bond pads are structured to be connected to external circuitry by solder bumps, and the special contact pads are not structured to be connected to external circuitry by solder bumps.

24. The integrated circuit of claim 8, wherein the bond pads are structured to be in electrical contact with a package for housing the integrated circuit, and the special contact pads are not structured to be in electrical contact with the package.

25. The integrated circuit of claim 8, wherein the plurality of circuits includes a first circuit and a second circuit having a redundant function of the first circuit, and wherein the special contact pads are disposed about the first and second circuits to communicate with the first and second circuits.

26. The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the first circuit if it is defective and for enabling the second circuit.

27. The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the second circuit.

28. The integrated circuit of claim 8, further comprising electrostatic discharge protection circuitry for the bond pads and not for the special contact pads.

29. An integrated circuit comprising:

a plurality of bond pads;

an internal circuit not directly monitorable by the bond pads; and

at least one special contact pad for directly accessing the internal circuit.

30. The integrated circuit of claim 29, wherein the internal circuit comprises an embedded memory array, and the at least one special contact pad communicates address and memory data with the embedded memory array.

31. The integrated circuit of claim 29, wherein the internal circuit comprises programmable circuitry, and the at least one special contact pad communicates programming signals to the programmable circuitry.

32. The integrated circuit of claim 29, wherein the bond pads are arranged in a first predetermined alignment and the at least one special contact pad is in a second predetermined alignment.

33. The integrated circuit of claim 29, wherein the at least one special contact pad is smaller than the bond pads.

34. The integrated circuit of claim 29, further comprising a spring contact element attached to the at least one special contact pad.

35 A package for housing an integrated circuit, comprising:

a plurality of terminals for testing the overall operation of the integrated circuit; and

a special contact pad for directly accessing an internal circuit of the integrated circuit.

36. The package of claim 35, wherein the special contact pad is for communicating test signals for the integrated circuit.

37. The package of claim 35, wherein the special contact pad is for communicating test signals from the integrated circuit.

38. The package of claim 35, wherein the contact pads are aligned in a grid pattern on the integrated circuit, and the special contact pads is not aligned in the grid pattern.

39. The package of claim 35, wherein the package comprises a ball-grid-array (BGA) package and the contact pads include contact balls.

40. The package of claim 35, wherein the special contact pad is smaller than the contact pad.

41. The package of claim 35, wherein the special contact pad has a maximum dimension of approximately 10 microns.

42. A method of testing circuitry in an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to the circuitry; and

monitoring an output of the circuitry through the special contact pad.

43. A method of testing circuitry in an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to the circuitry through the special contact pad; and

monitoring an output of the circuitry through the bond pad.

44. A method of testing an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to a first circuit through at least one of the bond pads;

monitoring an output of the first circuit through the special contact pad;

providing the output of the first circuit to a second circuit; and

providing an output of the second circuit to at least another one of the bond pads.

45. A method of testing an integrated circuit on a wafer, comprising:

electrically contacting a first test substrate to special contact pads disposed on the integrated circuit; and

electrically contacting a second test substrate to bond pads disposed on the integrated circuit.

46. A probe card comprising:

a first probe element for contacting bond pads of an integrated circuit; and

a second probe element for contacting a special contact pad of the integrated circuit

47. The probe card of claim 46, wherein the first and second probe elements comprise cantilevered probes.

48. The probe card of claim 46, wherein the first and second probe elements comprise contact balls.

49. The probe card of claim 46, further comprising a plurality of the first probe elements arranged in a first predetermined alignment, and wherein the second probe element is arranged in a second predetermined alignment.

50. The probe card of claim 49, wherein the predetermined alignment is a grid pattern.

51. The probe card of claim 49, wherein the predetermined alignment is a rectangular pattern.

52. The probe card of claim 49, wherein the first and second probe elements have different lengths.

53. The probe card of claim 49, wherein the first and second probe elements are spring contact elements.

54. The probe card of claim 53, wherein the spring contact elements include pyramid-shaped tip contact structures.

55. The probe card of claim 49, wherein the first and second probe elements are COBRA-style probes.

56. An apparatus for communicating signals with an internal circuit node and input/output (I/O) node of a semiconductor device, comprising:

a first contact element for communicating signals with the internal circuit node; and

a second contact element for communicating signals with the I/O node.

57. The apparatus of claim 56, wherein the first contact element comprises a resilient contact element.

58. The apparatus of claim 57, wherein the second contact element comprises a resilient contact element.

59. The apparatus of claim 56, wherein the first and second contact elements have different lengths.

60. A method of communicating a signal to an internal circuit node of a semiconductor device, comprising:

contacting a special contact pad that is electrically coupled to the internal circuit node; and

transferring electrical energy through the special contact pad to the internal circuit node.

61. A socket for releasably connecting a first electronic component to a second electronic component, comprising:

a first plurality of resilient contact structures extending upward from a top surface of a support substrate, the first plurality of resilient contact structures for communicating signals with a first plurality of contact points of the first electronic component;

a second plurality of resilient contact structures extending upward from the top surface of the support substrate, the second plurality of resilient contact structures for communicating signals with a second plurality of contact points of the second first electronic component; and

a plurality of contact structures disposed on a bottom surface of the support substrate, selected ones of the contact structures are connected through the support substrate to selected ones of the resilient contact structures.

62. The socket of claim 61, wherein the second electronic component is a circuit board.

63. The socket of claim 61, further comprising means for receiving the first electronic component.

64. The socket of claim 61, further comprising means for urging the first electronic component down onto the first and second resilient contact elements.